

## A 60 GHz GaAs FET AMPLIFIER

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Abstract

Using a  $1/4\mu\text{m}$  gate structure, a new millimeter wave FET device has been developed. This device, in a waveguide/MIC amplifier circuit, has demonstrated gains of  $5.0 \pm 0.5$  dB from 55 to 62 GHz with a minimum noise figure of 7.1 dB at 60 GHz.

Introduction

For millimeter wave applications requiring low noise solid state devices, three terminal devices such as GaAs FETs are desired as opposed to 2-terminal diode devices due to their low noise properties, inherent input/output isolation and suitability for GaAs monolithic circuit integration. Recent papers have reported an all FET receiver at 30 GHz,<sup>1</sup> FET amplifiers through 40 GHz<sup>2,3</sup> and a FET oscillator at 70 GHz.<sup>4</sup> This paper will present the first 60 GHz FET amplifiers.

Device Description

A direct write E-beam lithography system with a CAD pattern generator was used to design and fabricate the millimeter-wave FET devices<sup>5</sup>. SEM micrographs of the FET illustrating the device geometry and the channel structure are shown in Figure 1. The device geometry consists of two  $1/4 \times 30\mu\text{m}$  gate fingers in an interdigital structure with the source metallization pattern surrounding the active area. As shown in the figure, the gate is offset toward the source in the channel in order to reduce the source parasitic resistance. Both ion implanted (II) and vapor phase epitaxy (VPE) materials have been used to fabricate these devices.

Device Characterization

These devices were characterized by making DC measurements, 2 to 18 GHz S-parameter measurements and gain and noise figure measurements at 30 GHz. Based on the DC and S-parameter data, the device equivalent model was constructed which was then used to design the 30 GHz test amplifiers. These amplifiers were used to evaluate the gain and noise performance of the devices at high frequencies and confirm computations based on the device circuit model. Biased for maximum gain, these amplifiers demonstrated stable gains of 12 to 17 dB at 30 GHz. The input/output reflection coefficients were low and the gain response was smooth and relatively broadband indicating no tendency to oscillate. A total of 5 amplifiers, using devices from 4 different wafers, were measured at 30 GHz with a minimum measured MAG of 12 dB.

In addition to the gain measurements, a series of noise figure tests were performed on these amplifiers. The results of these 30 GHz tests together with the gain data are summarized in Table I. The best unit exhibited a 2.6 dB noise figure with 8.3 dB associated gain, and a minimum noise figure of 2.0 dB with 4.1 dB associated gain. It should be emphasized that this is amplifier data and that the device noise figure is lower. The results of these measurements and equivalent circuit modeling indicate that these FET devices would provide a gain of approximately 6 dB at 60 GHz with useful noise figures.

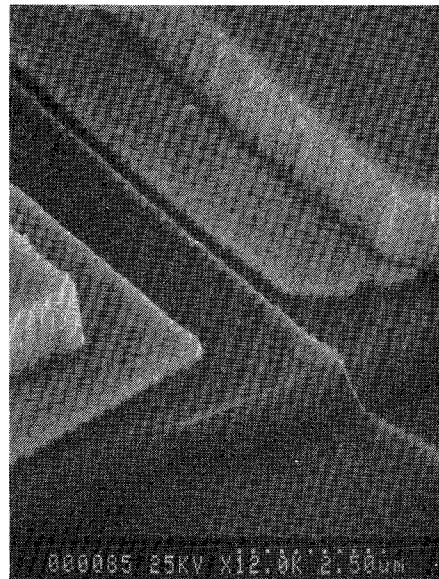
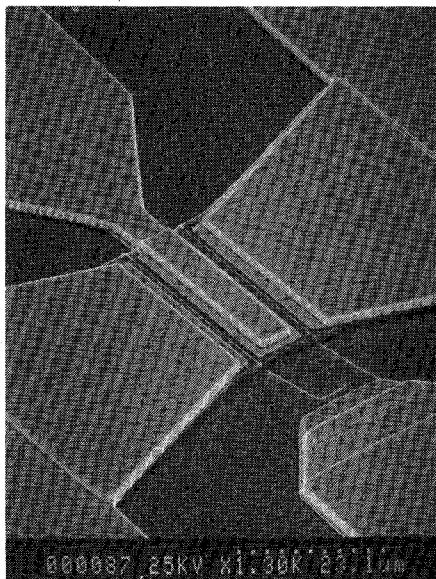


Figure 1 SEM of  $0.25 \times 60\mu\text{m}$  FET.

TABLE 1  
AMPLIFIER PERFORMANCE AT 30 GHz

Device Lot	Material	M.A.G. (dB)	Noise Figure (dB)	Associated Gain (dB)
DF04	II	12.5	3.5	7.7
DF05	II	12.0	2.8	8.1
DF06	VPE	17.0	3.5	7.7
DF07	VPE	17.0	2.6	8.3

60 GHz Amplifier Description

A 60 GHz integrated waveguide/MIC amplifier and test fixture were developed based on our previous Ka-band experience.<sup>2</sup> The fixturing hardware, illustrated in Figure 2, consists of a test base with V-band input/output E-plane bends, the waveguide/MIC amplifier wafer and the cover/backshort. The wafer, shown in Figure 3, contains the input and output waveguides and a channel 60 mils wide between them which forms a waveguide below cutoff. The FET and the MIC matching elements are mounted in this channel. The amplifiers were constructed using the two matching network topologies shown in Figure 4. The microstrip matching networks used series low impedance  $\lambda/4$  inverters to match the device input and output impedances. High and low impedance  $\lambda/4$  transmission line sections and chip capacitors were used for bias injection to the gate or drain. The prematched amplifiers employed shunt inductive elements, consisting of 0.7 mil bond wires and high dielectric constant chip capacitors, and  $50\Omega$  input/output lines. The best

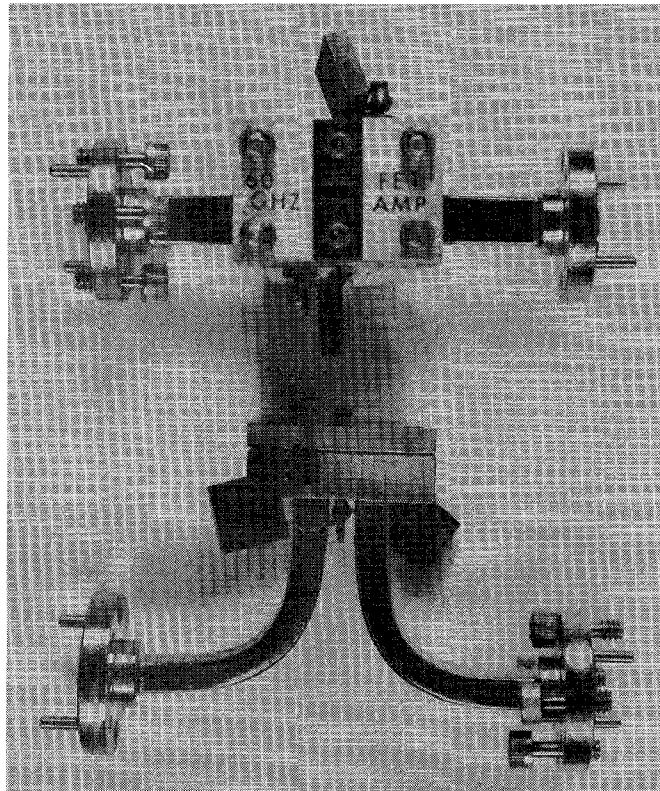


Figure 2 60 GHz FET amplifier and test fixture.

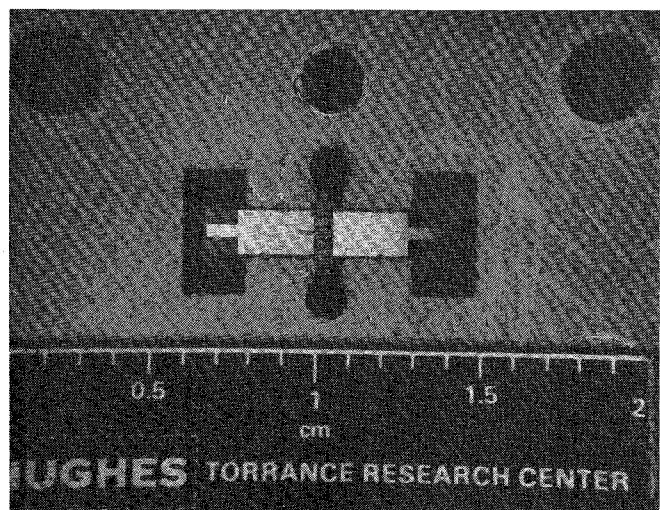
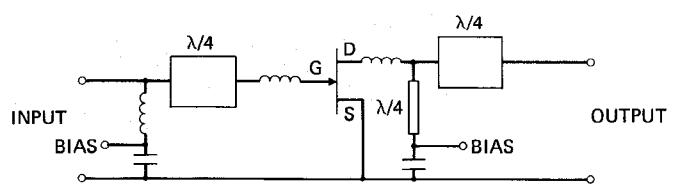


Figure 3 Photograph of 60 GHz MIC amplifier.

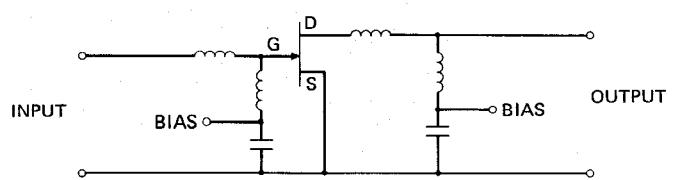
results to date were achieved with the prematched amplifiers. Both circuits were fabricated on 7 mil quartz substrates with CrAu metallizations and included a waveguide-to-microstrip transition. The amplifier wafer is Kovar with dimensions of 0.825x0.554x0.115 inches.

60 GHz Amplifier Performance

Using this approach, several FET amplifiers were fabricated and tested at 60 GHz. The frequency response of amplifier 2 is shown in Figure 5. The gain is  $5.0 \pm 0.5$  dB extending from 58 to 62 GHz. At 63 GHz the gain is 3.7 dB. The gain roll-off below 58 GHz and above 62 GHz is caused by the input matching network and not the FET device. The input return loss of this amplifier is greater than 15 dB at frequencies near 60 GHz but decreases rather abruptly below 58 GHz and above 60 GHz thereby creating the gain roll-off. The output return loss was only 3 to 5 dB across the band, indicating that by properly matching the output impedance, an additional gain of 2 to 3 dB can be achieved. Similar results were obtained with other devices from different wafers. The performance characteristics of the three amplifiers are summarized in Table 2. Amplifier 1 achieved the highest gain with a gain of  $5.5 \pm 0.5$  dB from 55 to 61 GHz.



(a) MICROSTRIP MATCHING NETWORK AMPLIFIER CONFIGURATION



(b) PREMATCHED FET AMPLIFIER CONFIGURATION

Figure 4 60 GHz amplifier configurations.

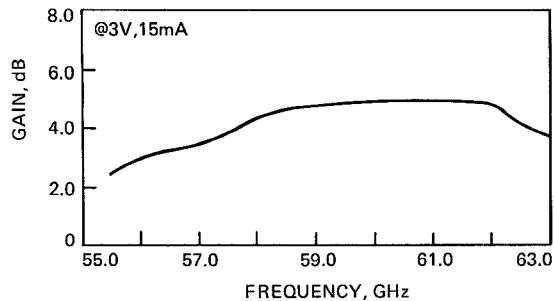


Figure 5 Frequency response of a 60 GHz FET amplifier.

TABLE 2  
60 GHz AMPLIFIER PERFORMANCE

Amplifier #	Device Lot	Gain (dB)	Frequency (GHz)	Output Power at 1 dB Compression* (dBm)
1	DF04	5.5 ± 0.5	55-61	+1.35
2	DF04	5.0 ± 0.5	58-62	+6.2
3	DF06	3.8 ± 0.5	55-60	—

\*at 60 GHz

The noise figure and associated gain of amplifier 2 is shown in Figure 6. At 60 GHz, as a function of drain bias, the noise figure ranged from 7.1 to 8.9 dB with an associated gain of 3.1 to 5.8 dB, respectively. The minimum noise measure, 9.5 dB, was achieved at  $I_D = 10$  mA with a noise figure and associated gain of 7.5 dB and 3.9 dB, respectively. The noise figure of the device is estimated to be ~5 dB. No attempts were made to optimize the amplifier for minimum noise figure.

The small signal gain compression characteristics of amplifiers 1 and 2 were measured at 60 GHz. The results are listed in Table 2. Biased at  $V_D = 3.0$  volts and  $I_{DSS}$  ( $V_G = 0$ ), amplifier 2 demonstrated 6.2 dBm output power with 4.1 dB gain at the 1 dB compression point.

#### Conclusions

FET devices operating as amplifiers have been demonstrated at 60 GHz. They represent the first reported FET amplifiers to operate at these frequencies and the first to employ the microstrip MIC format at 60 GHz. The key to these remarkable results is the 1/4 micron gate FET device. These results represent the initial and very successful thrust of GaAs FET technology into the millimeter wave spectrum.

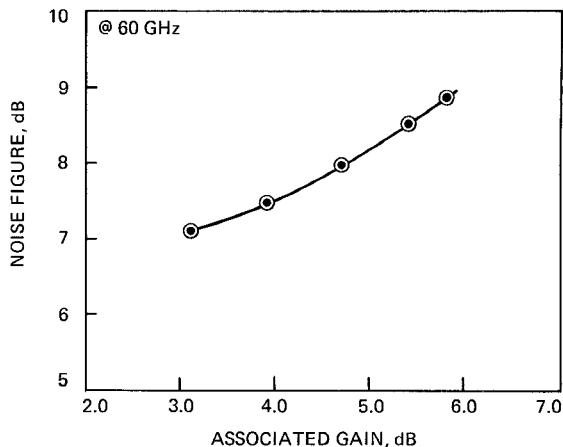


Figure 6 60 GHz FET amplifier noise figure and associated gain.

Until now, millimeter wave frequencies have been dominated by 2-terminal diode devices. However, with this achievement, we anticipate that FET devices, with their inherent low noise and 2-port properties, will advance to frequencies of 100 GHz and, perhaps, beyond.

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